

Appl. No. 10/681,399

Reply to Examiner's Action dated November 29, 2005

**IN THE CLAIMS:**

1. (Currently Amended) A method of fabricating a semiconductor device, the method comprising:  
forming a gate on a semiconductor substrate, the gate including opposing side surfaces;  
depositing an oxide material over the gate and, as well as over the semiconductor substrate and on a side of the gate, the opposing side surfaces of the gate being substantially free of the oxide material; and  
forming spacers on the opposing side surfaces of the gate, the spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.
2. (Original) The method of claim 1, the gate being doped with p-type or n-type dopant.
3. (Original) The method of claim 2, the sidewall spacers mitigating diffusion of dopants from the opposing side surfaces of the gate.
4. (Original) The method of claim 1, the oxide material being deposited by physical vapor deposition.
5. (Original) The method of claim 4, the physical vapor deposition method being anisotropic.
6. (Original) The method of claim 4, the physical vapor deposition method comprising at least one of a collimated sputtering method, a long throw sputtering method, or an ionized metal plasma sputtering method.
7. (Original) The method of claim 1, the oxide material comprising at least one of SiO<sub>2</sub>, AlO<sub>3</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub> (AlHf) O<sub>x</sub>, HfO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, silicon oxynitride, or hafnium silicon oxynitride.

Appl. No. 10/681,399

Reply to Examiner's Action dated November 29, 2005

8. (Original) The method of claim 1, the formation of the spacers further comprising providing a nitride layer over the gate after depositing the oxide material; and etching the nitride layer.

9. (Original) The method of claim 8, further comprising implanting an LDD implant after forming the gate, but before depositing the oxide layer; and implanting a source/drain implant after forming the nitride spacers.

10. (Original) The method of claim 9, the LDD implant and the source/drain implant forming a source region and a drain region of the semiconductor device.

11. (Original) The method of claim 10, the gate forming part of a p-type metal oxide semiconductor (PMOS) structure.

12. (Currently Amended) A method of fabricating a semiconductor device, the method comprising:

forming a gate on a semiconductor substrate, the gate being doped and including opposing side surfaces;

depositing an oxide material over the gate ~~and~~ as well as over the semiconductor substrate and on a side of the gate, the opposing side surfaces of the gate being substantially free of the oxide material;

forming a nitride layer over the gate and the oxide material; and

etching the nitride layer to form nitride spacers on the opposing side surfaces of the gate, the nitride spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.

Appl. No. 10/681,399

Reply to Examiner's Action dated November 29, 2005

13. (Original) The method of claim 12, the nitride spacers mitigating diffusion of dopants from the opposing side surfaces of the gate.

14. (Original) The method of claim 12, the oxide material being deposited by physical vapor deposition.

15. (Original) The method of claim 14, the physical vapor deposition method comprising at least one of a collimated sputtering method, a long throw sputtering method, or an ionized metal plasma sputtering method.

16. (Original) The method of claim 12, the oxide layer comprising at least one of  $\text{SiO}_2$ ,  $\text{AlO}_3$ ,  $\text{ZrO}_2$ ,  $\text{HfO}_2$  ( $\text{AlHf}$ )  $\text{O}_x$ ,  $\text{HfO}_2$ ,  $\text{La}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ , silicon oxynitride, or hafnium silicon oxynitride.

17. (Original) The method of claim 12, the gate comprising a polysilicon material doped with a p-type dopant.

18. (Original) The method of claim 12, further comprising: implanting a LDD implant after forming the gate, but before depositing the oxide layer; and implanting a source/drain implant after forming the nitride spacers.

19. (Original) The method of claim 12, the gate forming part of semiconductor device comprising a PMOS structure.

Claims 20-23 (Canceled)

24. (Currently Amended) The method of claim 1 wherein depositing an oxide material over the gate and, as well as over the semiconductor substrate and on a side of the gate, includes

Appl. No. 10/681,399

Reply to Examiner's Action dated November 29, 2005

depositing an oxide material directly on the gate and directly on the semiconductor substrate.

25. (Previously Presented) The method of claim 1 wherein forming a gate on a semiconductor substrate includes forming a conductive layer over the substrate, and patterning the conductive layer to form the gate.

26. (Currently Amended) The method of claim 12 wherein wherein depositing an oxide material over the gate and as well as over the semiconductor substrate and on a side of the gate, includes depositing an oxide material directly on the gate and directly on the semiconductor substrate.

27. (Previously Presented) The method of claim 12 wherein forming a gate on a semiconductor substrate includes forming a conductive layer over the substrate, and patterning the conductive layer to form the gate.